EEIE30069
VLSI TESTING AND DESIGN FOR TESTABILITY

Mango Chao (趙家佐)

Fall 2022

Administrative Matters

- **Time:** Thursday 789 (3:30pm~6:20pm)
- **Location:** all lectures will be given online! (official classroom EDB27)
- **Instructor:** Mango Chao (趙家佐)
- **Email:** mango@nycu.edu.tw
- **Office Hours:** Monday 1:30pm~3:30pm, made by appointment
- **Course website**
  - http://tiger.ee.nctu.edu.tw/course/Testing2022Fall/index.htm
  - Download lecture notes from E3 or course website
  - Lecture notes and assignments will be posted on course website
- **Teaching Assistants:**
  - Yu-Teng Nien (粘育騰) nien9304.ee05g@nctu.edu.tw
  - Vivian Wu (吳佩穎) higgsboson2314@gmail.com
  - No fixed office hours, made by appointment

Course Objective

- **To understand concepts of VLSI testing from an IC design house's point of view**
  - Especially designed for EDA students
  - If you are an EDA student and wants to work in a testing-related team in an IC design house, what do you need to know?
  - How EDA tools in testing area are designed
  - What's the impact of those EDA tools on digital IC design flow
- **Prerequisite**
  - Logic design
  - Basic VLSI design and synthesis flow
  - C/C++ programming

Covered Topics

- **Introduction to Test Process**
- **Logic Simulation**
- **Fault Modeling**
- **Fault Simulation**
- **Combinational ATPG (automatic test pattern generation)**
- **Testability Analysis**
- **Sequential ATPG**
- **Design for Testability (DfT)**
- **Built-in-self-test (BIST)**
- **On-chip Test Compression**

Assignments and Labs

- **7 homework assignments**
  - All programming
  - Based on a C++ code base provided by this course
  - You need to add new functions to this code base to complete each assignment
  - TA will introduce this code base to you today
  - Also, Assignment 0 will be given today and due in a week
  - If you cannot finish Assignment 0, you better drop this course
- **2 labs regarding DfT and ATPG**
  - Show you how to operate current commercial DfT and ATPG tools and their roles in the entire design flow
  - Need to go to a computer room of our institute
  - No computer room has enough seats for all current students
  - Need to figure a way out to accommodate all students…. will let you know later

Grading

- **Grading**
  - Midterm: 30%
  - Final: 30%
  - Assignment: 40%
  - Attendance doesn’t matter
- **Honor code**
  - Sign and turn in the honor code on E3 in the first week
    - otherwise you won’t get any score from this class
  - Any form of cheating is not allowed! (including assignments)
  - Total score will be 0 if you get caught
- **Exams**
  - Midterm: 11/3 (8^{th} week) or 11/10 (9^{th} week)
  - Final: 12/29 (16^{th} week) or 1/5 (17^{th} week)
  - Need to go to the classroom EDB27 (or another bigger one)

Textbook

- *VLSI Test Principles and Architectures* , Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, Morgan Kauffman 2006.
- *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits* , M. Bushnell and V. Agrawal, Kluwer Academic Publishers, 2000.
- *Testing of Digital Systems* , N. K. Jha and S. Gupta, Cambridge University Press, 2003.
- *Digital Systems Testing and Testable Design* , M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990.
  - Most of the material in this course comes from this one
  - There is a free pdf version that you can download online